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Method and Apparatus for Reducing Leakage in Integrated Circuits

Researchers at the University of South Florida have developed a method to reduce the leakage power in transistors called LECTOR (LEakage Control TransistOR) for designing CMOS circuits.

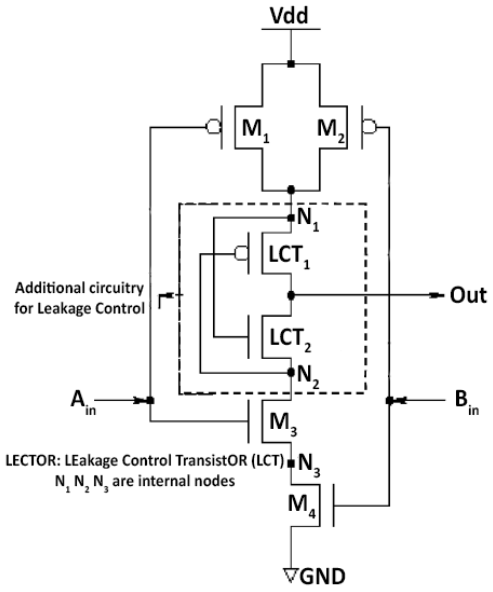
CMOS is a low power integrated circuit. Optimization of power in the CMOS circuit is critical. Leakage power is the undesired power that will cause power dissipation in the circuit. The scaling down of device dimensions, supply voltage, and threshold voltage for achieving high performance and low dynamic power dissipation has largely contributed to the increase in leakage power dissipation. An efficient design methodology is required to reduce the leakage power in CMOS circuits. The sleep signal controlled transistor can be used for the reduction in leakage power, but they require an additional circuit causing delay and area penalties. Hence, there is a need for reduction of leakage power without additional circuitry and to reduce the size of the transistor.

Researchers at USF have created a method that yields better leakage reduction in the CMOS circuit as the threshold voltage is decreased, which aids in further reduction of supply voltage and minimization of transistor sizes. Unlike other leakage control techniques, LECTOR does not need any control circuitry to monitor the states of the circuit. Hence, avoiding the sacrifice of obtained leakage power reduction in the form of dynamic power consumed by the additional circuitry to control the overall circuit states. The CMOS circuit has application in designs involving deep submicron and Nano technologies.

ADVANTAGES:

- **Reduction in leakage power**
- **No compensation of switching power**
- **Reduces footprint-trims additional circuitry**

Minimization of Transistor Sizes In CMOS Circuit



Schematic of Leakage Reduction Circuit

Tech ID # 03B095 **Patent #: 7,256,608**

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