

Method for the Assembly of Nanowire Interconnects

Researchers at the University of South Florida have invented a method for the synthesis of nanowires in a silicon nanoporous template by electrode position, and a novel technique for the integration of nanowires to transduction surfaces.

Sensors based on metallic nanowires, nanorods and nanoparticles are being investigated because of unique electronic, optical, biological and magnetic sensing properties that these nanostructures offer. It is generally known that nanowires are synthesized using electroplating. As devices continue to be scaled down, the contact pad area also shrinks, which requires further reductions in the interconnect dimensions. Synthesized nanowires are used to provide improved packaging and interconnect schemes for integrated circuits and sensors. In particular, the fabrication of through-wafer nanowires to provide vertical interconnects in 3D devices requires the realization of high-density circuits and systems. There has been difficulty in handling the nanowires and functionalization of the sensing elements with nanowires.

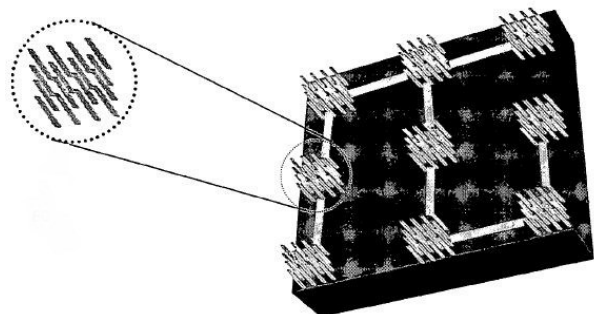
Accordingly, an improved method is required for the synthesis and assembly of ultra-high aspect ratio metallic nanowires, which are to be deployed as interconnects and sensing elements.

The present technology provides a method for the synthesis of nanowires in a silicon nanoporous template by electrode position, and a novel technique for the integration of nanowires to transduction surfaces. Thereby providing a generic, high density, reconfigurable and low cost alternative to conventional packaging schemes.

ADVANTAGES:

- Ability to easily control the size and shape and morphology of nanowires
- Elegant alternative to molecular beam epitaxy and microlithography
- High density, reconfigurable and low cost
- Synthesis of long wires (>100 microns)
- Capable of large scale assembly compared to microfluidics

Nanowires Synthesis in a Silicon Nanoporous Template



Exemplary Placement of Nanowires on a Receiving Silicon Substrate

Tech ID # 03B104

Patent #: [7,112,525](#)