Researchers at the University of South Florida have developed a method and apparatus to build wide operating, low-power and robust level-shifter for memory and standalone applications.

Microprocessors can include multiple components parts, such as execution units, memory, and decoders. Each of the component parts can operate at different supply voltages. For example, execution units can require higher supply voltages relative to decoders. As such, execution units can consume more power than decoders consume. When component parts operating with different voltage supplies communicate with each other, the communication signals can create static current in the system. Voltage level shifters (LS) can be used in systems where component parts operating with different voltage supplies must communicate with each other. Level shifters can be applied to an embedded dynamic random access memories (eDRAM) where LS is employed in the wordline path. The thorough investigation reveals that leakage power of LS can pose a serious threat by lowering the wordline voltage and subsequently affecting the speed and retention time of eDRAM. Furthermore, the delay of LS under worse case process corners can cause functional discrepancies.

USF inventors have proposed novel low overhead, power gated, pulsed level shifters, to break the dependency of LS speed on charge pump (CP) output variation and enable fast level conversion and higher retention time. The system level simulation indicated the presence of an interesting tradeoff between bandwidth, leakage power of LS and standby power of system that is governed by retention time. Lastly, using the new pulsing technique, new self-collapsing LS’s that are needed at voltage domain interfaces were developed. The self-collapsing LS provides fast level conversion compared to conventional LS with small power overhead.

Tech ID # 14A065 Patent # 9,673,821