Researchers at the University of South Florida have developed a method of improving the reliability of integrated circuits while providing chip level diagnostics and prognostics, and observing chip level faults off chip, using a fraction of the area overhead previously required.

Continuing advances in semiconductor technology have resulted in ever decreasing size of transistors allowing more to be packed on a single chip. However, as the number of transistors and gates increases, the complexity, elevated current levels, fault classes, and limited access to internal nodes makes detecting reliability faults increasingly more costly.

Present day failure mechanisms in popular integrated circuit process nodes include negative bias temperature instability (NBTI), hot carrier injection (HCI), electromigration, process parameter variation, subthreshold leakage, and reduced reliability due to radiation effects. These failure mechanisms manifest as unique quiescent power supply current signatures.

This novel method developed at the University of South Florida complements embedded testing including boundary scan and built in self test (BIST) while providing a transparent method of propagating faults off-chip without the need for bit error lines or any additional signal overhead. The method is based on a built-in current sensor approach that includes a low overhead method of propagating faults using dedicated or shared VDD supply nets. Faulty quiescent current information propagated off chip can be used to detect a broad class of quiescent current related defects as well as providing diagnostics information. Defect detection and diagnostics information is automatically mapped to a suspect partition that includes the faulty circuit(s).

This method is compatible with any CMOS process in application specific integrated circuits (ASICs) and field programmable gate arrays (FPGAs) and has been demonstrated in prototypes fabricated in a 180nm commercial CMOS process. The prototypes were characterized under extreme conditions including Cobalt-60 radiation for total ionizing dose.

The USF IP can be easily included in a company’s standard cell or custom IP library and presents minimal impact on floorplanning, placement, or routing. This innovative technique provides a cost effective solution for propagating faults off chip and complements BIST, boundary scan, and existing chip level defect detection, diagnostic, and prognostic techniques.